Central Glass & Ceramic Research Institute
KOLKATA (WEST BENGAL) INDIA
CORRIGENDUM

REFERENCE NO. :- P/NC/323/DK/SO(SB)/OTE/20-21 DATE: 25/03/2021

NAME OF EQUIPMENT: DEVELOPMENT AND SUPPLY OF INTERFACE BOARD FOR CCD BASED FBG INTERROGATION

NOTE: The Bids must be submitted in the Central Public Procurement Portal (URL:https://etenders.gov.in/eprocure/app) only. Manual/Offline bids shall not be accepted under any circumstances. Bidders should quote in INR only.

CONSEQUENT TO THE PRE-BID MEETING HELD ON 12/03/2021, THE REVISED SPECIFICATION IS GIVEN BELOW:-

SPECIFICATIONS:-

Details of Items*	Quantity
1.End Use :R&D consumable at CGCRI 2. Detailed specification: **Development and Supply of** **Interface Board for CCD based FBG Interrogator (CCD based OEM module will be supplied by CGCRI)** *[Hardware modules along with GUI(source code included in Python/C#) and FPGA project file(source code included in VHDL/Verilog) are to be delivered]* • Compatibility required with both 256px and 512px CCDOEM • No. of multiplexed FBG Sensors to be monitored : 16 • Wavelength Repeatability / Accuracy: +/- 5pm • Resolution: 16 bit • Scan Speed: 3KHz • Clock Speed for driving: 5MHz • Exposure time : 10 to 200000 clock cycles (should be configurable from GUI software) • Communication interface: Ethernet • Noise Level: less than -60dBm • Operational Endurance: Reliability of 24X7 continuous operation for at-least 1 year • Power Supply: 5VDC • Operating Temperature :≤10°C to ≥40°C • Storage Temperature :≤0°C to ≥65°C 3. Scope of supply & incidental services:Opto-Electronic Componentmanufacturer matching the conditions of Annex 2 , servicing required for three years 4. Inspection and Tests required:Yes 5.Acceptance test: verification of the component as per specifications 6.Qualification criteria if any:Items should match with the stated specifications Note: detailed specifications in Annexure 1	5no.s

25/3/21
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Annexure 1
Detail description of work

1. Scope

Scope of this project to develop an interface card for CCD based OEM Spectrometer (that will be supplied by CGCRI) to read linear detector array and send pixel data over Ethernet interface. Interface Board may be planned as two separate boards namely a Sensor Carrier Board and FPGA Board.

2. Product details and Requirements by CGCRI

An Interface board is to be developed for CCD based OEM interrogator that uses standard InGaAs Sensor array. The board is intended to use for converting analog pixel data to digital and send the digital pixel data to an external devise through Ethernet.

	Feature / Parameter of Interface card	Specifications
1.	Communication Interface	Ethernet (1 Gbps)
2.	Clock Frequency	Fixed, 5 MHz
3.	Configurable features	Exposure Time ▪ (Pulse width &Delay time) User configurable ADC parameters ▪ ADC Gain ▪ ADC Offset voltage

3. Model Architecture for Interface board

The model solution is based on a Sensor Carrier Board to mount CCD based OEM and ADC. This board is responsible for interfacing with the sensor array and provides control signals like clock, RESET etc. It also interfaces with ADC that converts the analog pixel data from the sensor. The digital data from the ADC card, is then packetized and sent through 1 Gbit Ethernet in TCP/IP format by the FPGA board.

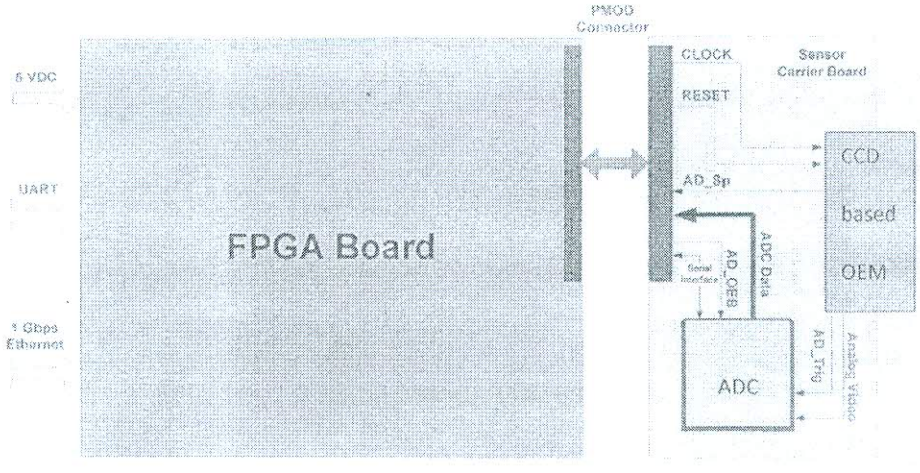

Figure: 1 Interface Board Functional Block Diagram

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The following are the functionalities of FPGA Board:

- Communicate with InGaAs detector array through GPIO as per its protocol.
  a. Generate digital signals such as ADC clock, 'Exposure Time' signal, Reset Signal.
- Communicate with ADC through serial interface.
- Read parallel data lines from ADC at specific intervals
- Packetize the ADC data as per Ethernet frame format
- Send the digital pixel data to an external devise through Ethernet interface.
- Retrieve following 'configurable parameters' from Ethernet data frame received from an external device.
  a. Exposure Time
  b. ADC parameters like user programmable gain & user programmable offset voltage
- Perform configuration settings as per the commands received through Ethernet.
- Communicate with external devise through UART interface for configuring Ethernet IP & Portas an initial set up.
- UDP will be used as the protocol for Ethernet communication.

Detector Array Description:

The detector is an array of 256 or 512 pixels of InGaAs linear image sensors which is referred to as CCD 256OEM (for 256 pixel version) and CCD 512OEM (for 512 pixel version). These OEM modules have one fiber optic input and 22 electrical pins. The main control signals are:

1.	CLK	: 5MHz digital Input
2.	RESET	: Digital Input Pulse
3.	AD_sp	: Digital Output Pulse
4.	AD_trig	: Digital Output Pulse
5.	VIDEO	: Analog Pixel Data Output

CLK: The OEM module has to be driven with a high speed clock of 50% duty cycle. The frequency of the clock signal can be 5MHz.

RESET: This is a Digital Pulse in sync with the CLK signal. The RESET is high for an integral number of CLK cycles and Low for another integral number of CLK cycles. When the pulse is high, the pixels absorb photons from the optical input and this duration is called the Exposure Time or Integration Time.

AD_sp & AD_trig: After the Reset Signal is made Low, after a few CLK cycles, the OEM gives out a digital pulse signal AD_sp spanning several CLK cycles. This marks the starting pulse for pixel read out. After the AD_sp pulse ends, with every CLK cycle, the OEM gives out a narrow pulse on the AD_trig pin.

VIDEO: After the AD_sp pulse ends with every CLK cycle, the OEM gives out an analog voltage corresponding to each pixel in the pixel array of the OEM on the VIDEO pin. This is captured on an ADC and the digitized data has to be stored for each pixel. This set of 256 or 512 pixel data is called a 'Frame'.

The timing diagram of the system function is as shown below.

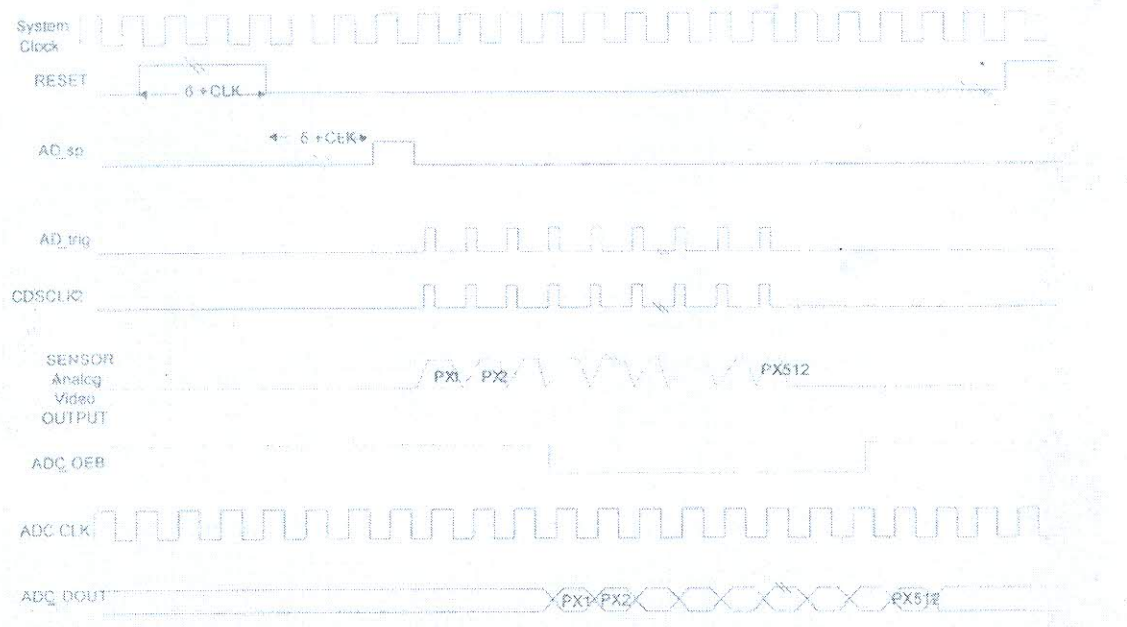

Figure 2: Timing Diagram

The ADC_CLK is same as the sensor clock. The RESET signal is made high for 6+ clock cycles and the logic waits for receiving the AD_sp signal which indicates the conversion start. After AD_sp signal, AD_trig signal is obtained corresponding to every pixel analog data. After the pixel data is made available at the ADC input, parallel digital data is received at every clock cycle for 512 pixels. ADC_OEB signal, which is the output enable, is made low for enabling the output. Selection of ADC operating mode, setting ADC Gain, offset are done through serial interface. Digital pixel data from ADC is read by FPGA and packetized as per Ethernet frame format. UART interface to FPGA is used for configuring IP address and port.

Annexure 2

The bidder should satisfy the following conditions:

1. The bidder should have in-house electronics manufacturing facility of SMT assembly line with optical inspection systems.

2. The bidder should have in-house optical component and system testing facilities comprising of facilities like Optical Spectrum Analyzer, Broadband Optical Source, Optical Circulators and Switches etc

3. The bidder should have prior experience in executing projects of optical sensor interrogation systems based on FPGAs.

4. The bidder firm should have DSIR approval.

The above amendments shall amount to amendments of the relevant terms of our Bid Document for CGCRI Tender No. P/NC/323/DK/SO(SB)/OTE/20-21.

All other Tender terms and conditions remain unchanged.

Bidders should quote only in INR.

25/3/24

(R. Ray)
Controller of Stores & Purchase

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आर. रे / R. Ray
भण्डार एवं क्रय नियंत्रक
CONTROLLER OF STORES & PURCHASE